CH# 2
Overview Of Hardware Description Languages
library IEEE;
use IEEE.STD_LOGIC_1164.all;

entity even_detector is
  port (a : in std_logic_vector(2 downto 0);
       even: out std_logic);
end even_detector;

architecture pos_arch of even_detector is
  signal s1, s2, s3, s4 : std_logic;
begin
  even <= (s1 and s2) and (s3 and s4);
  s1 <= (not a(2)) or (not a(1)) or (not a(0));
  s2 <= (not a(2)) or a(1) or a(0);
  s3 <= a(2) or (not a(1)) or a(0);
  s4 <= a(2) or a(1) or (not a(0));
end pos_arch;
Problem 2.5

Problem 2.6 (HW)

Problem 2.7
Problem 2.10

- **sop_arch**: use 2⁹ product terms (i.e., 2⁹ statements).
- **xor_arch**: modify the “odd <= . . .” statement to include xor operation on 10 signals.
- **str_arch**: use 9 component instantiation statements to instantiate 9 xor gates.
- **beh1_arch**: change the loop index from 2 to 9.
- **beh2_arch**: change the loop index from 2 to 9.