Chapter 4

BJT BIASING CIRCUIT
Introduction – Biasing

The analysis or design of a transistor amplifier requires knowledge of both the dc and ac response of the system. In fact, the amplifier increases the strength of a weak signal by transferring the energy from the applied DC source to the weak input ac signal. The analysis or design of any electronic amplifier therefore has two components:

• The dc portion and
• The ac portion

During the design stage, the choice of parameters for the required dc levels will affect the ac response.

What is biasing circuit?

Biasing: Application of dc voltages to establish a fixed level of current and voltage.
Purpose of the DC biasing circuit

• To turn the device “ON”
• To place it in operation in the region of its characteristic where the device operates most linearly.
• Proper biasing circuit which it operate in linear region and circuit have centered Q-point or midpoint biased
• Improper biasing cause
  • Distortion in the output signal
  • Produce limited or clipped at output signal

Important basic relationship

\[ I_E = I_C + I_B \]
\[ \beta = \frac{I_C}{I_B} \]
\[ I_E = (\beta + 1)I_B \approx I_C \]
\[ V_{CB} = V_{CE} - V_{BE} \]
Operating Point

- **Active or Linear Region Operation**
  - Base – Emitter junction is forward biased
  - Base – Collector junction is reverse biased
  - Good operating point

- **Saturation Region Operation**
  - Base – Emitter junction is forward biased
  - Base – Collector junction is forward biased

- **Cutoff Region Operation**
  - Base – Emitter junction is reverse biased
BJT Analysis

DC analysis
- Calculate the DC Q-point
  - solving input and output loops

AC analysis
- Calculate gains of the amplifier
  - Graphical Method

DC Biasing Circuits
- Fixed-bias circuit
- Emitter-stabilized bias circuit
- Collector-emitter loop
- Voltage divider bias circuit
- DC bias with voltage feedback
FIXED BIASES CIRCUIT

- This is common emitter (CE) configuration
- 1\(^{st}\) step: Locate capacitors and replace them with an open circuit
- 2\(^{nd}\) step: Locate 2 main loops which;
  - BE loop (input loop)
  - CE loop (output loop)
• **1**\textsuperscript{st} **step**: Locate capacitors and replace them with an open circuit
• **2\textsuperscript{nd} step**: Locate 2 main loops.
**BE Loop Analysis**

From KVL:

\[-V_{CC} + I_B R_B + V_{BE} = 0\]

\[\therefore I_B = \frac{V_{CC} - V_{BE}}{R_B}\]
• **CE Loop Analysis**

- From KVL;
  
  \[-V_{CC} + I_C R_C + V_{CE} = 0\]
  
  \[\therefore V_{CE} = V_{CC} - I_C R_C\]

- As we known;

  \[I_C = \beta I_B\]  \(\text{B}\)

- Substituting (A) with (B)

  \[I_C = \beta_{DC} \left( \frac{V_{CC} - V_{BE}}{R_B} \right)\]

Note that \(R_C\) does not affect the value of \(I_C\)
FIXED BIAS CIRCUIT

• DISADVANTAGE
  ➢ Unstable – because it is too dependent on $\beta$ and produce width change of Q-point
  ➢ For improved bias stability, add emitter resistor to dc bias.
Load line analysis

- A fixed bias circuit with given values of $V_{CC}$, $R_C$ and $R_B$ can be analyzed (means, determining the values of $I_{BQ}$, $I_{CQ}$ and $V_{CEQ}$) using the concept of load line also.

- Here the input loop KVL equation is not used for the purpose of analysis, instead, the output characteristics of the transistor used in the given circuit and output loop KVL equation are made use of.
Plot load line equation

\[ V_{CE} = V_{CC} - I_C R_C \]

IC(sat) occurs when transistor operating in saturation region

\[ I_{C_{sat}} = \frac{V_{CC}}{R_C} \mid V_{CE} = 0 \]

VCE(off) occurs when transistor operating in cut-off region

\[ V_{CE_{(off)}} = V_{CC} - I_C R_C \mid I_C = 0 \]
Circuit Values Affect the Q-Point

- Decreasing $V_{cc}$
- Increasing $R_c$
- Varying $I_b$
An emitter resistor, $R_E$ is added to improve stability.

1st step: Locate capacitors and replace them with an open circuit.

2nd step: Locate 2 main loops which:
- BE loop
- CE loop
EMITTER-STABILIZED BIAS CIRCUIT

1st step: Locate capacitors and replace them with an open circuit
EMITTER-STABILIZED BIAS CIRCUIT

- 2nd step: Locate 2 main loops.

BE Loop

CE Loop
EMITTER-STABILIZED BIAS CIRCUIT

• BE Loop Analysis

- From kvl;
  \[-V_{CC} + I_B R_B + V_{BE} + I_E R_E = 0\]
  Recall; \[I_E = (\beta + 1)I_B\]
  Substitute for \(I_E\)
  \[-V_{CC} + I_B R_B + V_{BE} + (\beta + 1)I_B R_E = 0\]
  \[\therefore I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E}\]
**EMITTER-STABILIZED BIAS CIRCUIT**

- **CE Loop Analysis**

  - From KVL;
    \[-V_{CC} + I_C R_C + V_{CE} + I_E R_E = 0\]
  - Assume;
    \[I_E \approx I_C\]
  - Therefore;
    \[V_{CE} = V_{CC} - I_C (R_C + R_E)\]
Improved Bias Stability

The addition of the emitter resistor to the dc bias of the BJT provides improved stability, that is, the dc bias currents and voltages remain closer to where they were set by the circuit when outside conditions, such as temperature, and transistor beta, change.

Without Re

\[ I_c = \left( \frac{V_{CC} - V_{BE}}{R_B} \right) \beta \]

With Re

\[ I_c = \left( \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E} \right) \beta \]

Note: It seems that beta in numerator canceled with beta in denominator.
VOLTAGE DIVIDER BIAS CIRCUIT

- Provides good Q-point stability with a single polarity supply voltage
- This is the biasing circuit wherein, ICQ and VCEQ are almost independent of beta.
- The level of IBQ will change with beta so as to maintain the values of ICQ and VCEQ almost same, thus maintaining the stability of Q point.
- Two methods of analyzing a voltage divider bias circuit are:
  - **Exact method**: can be applied to any voltage divider circuit
  - **Approximate method**: direct method, saves time and energy,
- 1st step: Locate capacitors and replace them with an open circuit
- 2nd step: Simplified circuit using Thevenin Theorem
- 3rd step: Locate 2 main loops which;
  - BE loop
  - CE loop
2nd step: Simplified circuit using Thevenin Theorem

From Thevenin Theorem:

$$R_{TH} = R_1 \parallel R_2 = \frac{R_1 \times R_2}{R_1 + R_2}$$

$$V_{TH} = \frac{R_2}{R_1 + R_2} V_{CC}$$
VOLTAGE DIVIDER BIAS CIRCUIT

- **2nd step**: Locate 2 main loops.
**VOLTAGE DIVIDER BIAS CIRCUIT**

- **BE Loop Analysis**

  - From KVL;
    
    \[-V_{TH} + I_B R_{TH} + V_{BE} + I_E R_E = 0\]
    
    Recall; \(I_E = (\beta + 1)I_B\)
    
    Substitute for \(I_E\)
    
    \[-V_{TH} + I_B R_{TH} + V_{BE} + (\beta + 1)I_B R_E = 0\]
    
    \[\therefore I_B = \frac{V_{TH} - V_{BE}}{R_{RTH} + (\beta + 1)R_E}\]
VOLTAGE DIVIDER BIAS CIRCUIT

- CE Loop Analysis

- From KVL;
  \[-V_{CC} + I_C R_C + V_{CE} + I_E R_E = 0\]

- Assume;
  \[I_E \approx I_C\]

- Therefore;
  \[\therefore V_{CE} = V_{CC} - I_C (R_C + R_E)\]
Approximate analysis:

\[ R_i \gg R_2 \rightarrow I_{R_2} \gg I_b \]

\[ (\beta + 1)R_E \gg R_2 \Rightarrow \beta R_E > 10R_2 \]

- If this condition applied then you can use approximation method.
- This makes \( I_B \) to be negligible. Thus \( I_1 \) through \( R_1 \) is almost same as the current \( I_2 \) through \( R_2 \). Thus \( R_1 \) and \( R_2 \) can be considered as in series. Voltage divider can be applied to find the voltage across \( R_2 \) (\( V_B \)).
Approximate Analysis

When $\beta R_E > 10R_2$, then $I_B \ll I_2$ and $I_1 \cong I_2$:

$$V_B = \frac{R_2 V_{CC}}{R_1 + R_2} \quad V_E = V_B - V_{BE}$$

$$I_E = \frac{V_E}{R_E}$$

From Kirchhoff’s voltage law:

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

$$I_E \cong I_C$$

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

This is a very stable bias circuit. The currents and voltages are nearly independent of any variations in $\beta$. 
Another way to improve the stability of a bias circuit is to add a feedback path from collector to base.

In this bias circuit the Q-point is only slightly dependent on the transistor beta, $\beta$. 
Base-Emitter Loop

From Kirchhoff’s voltage law:

\[-V_{CC} + I'_C R_C + I_B R_B + V_{BE} + I_E R_E = 0\]

Where \(I_B \ll I_C\):

\[I'_C = I_C + I_B \approx I_C\]

Knowing \(I_C = \beta I_B\) and \(I_E \approx I_C\), the loop equation becomes:

\[V_{CC} - \beta I_B R_C - I_B R_B - V_{BE} - \beta I_B R_E = 0\]

Solving for \(I_B\):

\[I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta(R_C + R_E)}\]
Applying Kirchoff’s voltage law:

\[ I_E + V_{CE} + I'_C R_C - V_{CC} = 0 \]

Since \( I'_C \cong I_C \) and \( I_C = \beta I_B \):

\[ I_C (R_C + R_E) + V_{CE} - V_{CC} = 0 \]

Solving for \( V_{CE} \):

\[ V_{CE} = V_{CC} - I_C (R_C + R_E) \]
Problem-Solving Technique: Bipolar DC analysis

Before analyzing we need to know the mode of operation.

If the mode of operation is not obvious → guess

1 - assume that the transistor is biased in the forward-active mode in which case

\[ V_{BE} = V_{BE(on)} = 0.7 \text{, } I_B > 0 \text{, } I_C = eta I_B \]

2 - analyze the circuit with this assumption

3 - evaluate the resulting state of the transistor.

If the initial assumed parameter values and

\[ V_{CE} > V_{CE(sat)} \]

are true, then the initial assumption is correct. However if

\[ I_B < 0 \]

then the transistor is probably cut-off

and if \[ V_{CE} < 0 \] the transistor is likely in saturation.

4 - If the initial assumption is proven incorrect
then a new assumption must be made and
the new circuit must be analyzed. Step 3 must then be repeated.

編號: @active@active

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(1)
<table>
<thead>
<tr>
<th>Mode</th>
<th>Active</th>
<th>Saturation</th>
<th>Cut-off</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$I_C = \beta I_B$</td>
<td>$I_C &lt; \beta I_B$</td>
<td>$I_B = I_C = I_E = 0$</td>
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<tr>
<td></td>
<td>$V_{BE} = 0.7$</td>
<td>$V_{BE} = 0.7$</td>
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<td></td>
<td>all the currents are positive</td>
<td>$V_{CE} &lt; 0$ or $0.2$</td>
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$$I_E = I_B + I_C$$

Example 1: $V_{BE} = 0.7$, $\beta = 100$ Find $Q$ point

Assume active 1

$$I_B = \frac{0.7 + 5}{10k + (\beta + 1)5k} = 8.35 \text{ mA}$$

$$I_C = \beta I_B = 0.835 \text{ mA}$$

$$I_E = (\beta + 1)I_B = 8.48 \text{ mA}$$

$$I_C = I_1 - I_L$$

$$1.835 \text{ mA} = \frac{12 - V_0}{5k} - \frac{V_0}{5k} \Rightarrow V_0 = 3.91$$

$$I_1 = 1.62 \text{ mA}, I_L = 1.782 \text{ mA}$$

$$V_{CE} = V_0 + 5 - I_E R_E = 4.7 > 0 \Rightarrow \text{Active}$$

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[Equations and graphs for circuit analysis and calculations are shown on the page.]
\( V_{BE} = 0.7, \beta = 100 \) find Q point, \( I_L \)

\[
V_{TH} = 12 \times 5k \times 6 \quad 10k
\]
\[R_{AC} = \frac{5k}{1.5k} = 2.5k\]

\[
V_{TH} = 6
\]
\[R_{AC} = 2.5k\]

\[
I_B = \frac{0 - 1.745}{10k + (\beta+1)5k} = 8.35 \, mA
\]

\[
I_C = \beta I_B = 100 \times 8.35 \, mA = 835 \, mA
\]

\[
I_E = (\beta+1)I_B = 843 \, mA
\]

\[-6 + I_C \times R_{TH} + V_{CE} + 5k \times I_E = 5 = 0\]

\[
V_{CE} = 11 - 1835 \, mA \times 2.5k - 5k \times 843 \, mA = 4.69
\]

\[
V_{CE} = V_C - V_E \quad V_C = V_{CE} + V_E
\]

\[
V_E = -5 + 5k \times I_E = -1.785
\]

\[
I_C = 3.915
\]

\[
I_L = \frac{3.915}{5k} = 0.782 \, mA
\]
\( V_b = 1 \), find \( V_c, \beta, \alpha \)

\[ I_b = \frac{V_b - 1}{100 \times 10^3} = 10 \mu A \]

\[ I_e = V_{BE} = -1.7, \quad V_b = 1 \]

\[ V_{BE} = V_b - V_E \]

\[ V_E = 1.7 \]

\[ I_e = \frac{10 - 1.7}{5k} = 1.66 \text{ mA} \]

\[ I_e = (\beta + 1) I_b \Rightarrow \beta + 1 = 160 \]

\[ \beta = 165 \]

\[ \alpha = \frac{1}{\beta + 1} = 0.994 \]

\[ I_c = \beta I_b = 165 \times 10 \times 10^{-6} = 1.65 \text{ mA} \]

\[ V_c = V_c = -10 + 5k \times 1.65 \times 10^{-3} = -1.7 \text{ volt} \]
Example: If $\beta = 100$, $V_{BE} = 0.7$, $V_{CE} = 5$, find Q point. If $V_S = 3$

Assume active.

$V_{BE} = 0.7$

$V_B = 1.7$

$I_1 = \frac{V_S - V_B}{15} = 1.53 \text{ m}$

$I_2 = \frac{17 + 12}{100} = 1.27 \text{ m}$

$I_b = I_1 - I_2 = 1.53 \text{ m} - 1.27 = 0.26 \text{ m}$

$I_c = \beta I_b = 100 \times 0.26 \times 10^3 = 2.6 \text{ m}$

$V_{CE} = 5 - 2.2 \times 2.6 = -1.72$

\[ V_{CE} < V_{CE} \text{ sat} \Rightarrow \text{ our assumption is wrong.} \]

Resolve (transistor in saturation).

$V_{CE} = V_{CE} \text{ (sat)} = 2$

$I_{c, \text{ sat}} = \frac{5 - 2}{2.2} = 2.182 \text{ mA}$.
Example:

Find $V_o$, $P_Z$

$V_o = V_b - V_{BE} = 10.7 - 1.7 = 10$

$I_L = \frac{10}{1.8 \times 10^3} = 5.55 \text{ mA}$

$I_R = \frac{22 - 10.7}{1.2k} = 9.416 \text{ mA}$

$I_C = I_E = 5.55 \text{ mA}$

$I_B = \frac{I_C}{\beta} = \frac{5.55 \times 10^{-3}}{150} = 37 \text{ mA}$

$I_Z = I_R - I_B = 9.416 \times 10^{-3} - 37 \times 10^{-6} = 9.379 \text{ mA}$

$P_Z = 10.7 \times 9.379 \text{ mW} = 100.36 \text{ mW}$
Example: find Q point, \( V_C, V_E, V_B \)
assume active.

\[ V_E = 0 \Rightarrow V_{EB} = 1.7 \]

\[ V_E - V_B = 7 \Rightarrow V_B = -1.7 \]

\[ I_b = I_2 - I_1 = \frac{-1.7 + 10}{10k} - \frac{10 + 7}{10k} = 0.09 \Rightarrow I_b = -10 \mu A \]

\[ I_b = -10 \mu A \Rightarrow \times \text{ wrong assumption} \]

The transistor is cut-off.

\[ I_b = 0, \quad I_C = 0, \quad I_E = 0, \quad V_E = 0, \quad V_C = -10, \quad V_B = 0 \]

Example: find Q point
assume active.

\[-10 + 2k I_E + 10k I_b + (-7 + 1k) I_E = 0\]

\[ I_E = (\beta + 1) I_b \]

\[ I_b = \frac{10 - 7}{10k + (\beta + 1)(1k + 1k)} = 0.023 \text{ mA} \]

\[ I_C = \beta I_b = 2.3 \text{ mA} \]

\[ I_E = 2.33 \text{ mA} \]

\[ V_{CE} = 10 - 2.3 \times 3 = 3.1 \Rightarrow V_{CE} (sat) \]

\[ V_B < V_C \Rightarrow \text{ transistor is cut-off} \]
Example: find $\Phi$

\[ I_1 = I_b + 20 \text{mA} \]
\[-10 + 10k (I_t + I_c) + 100k \times I_t + 7.5 \]
\[-10 + 10k (I_b + 20 \text{mA} + \beta I_b) + 100k (I_b + 20 \text{mA}) \]
\[ + 17 = 0 \]

\[ I_b = \frac{10 - 17 - 110k \times 20 \text{mA}}{10k + \beta \times 10k + 100k} \]
\[ = 1.163 \times 10^{-5} \]

\[ I_c = 1.582 \text{m} \]
\[ I_t = 1.316 \text{mA} \]

\[ V_{CE} = 10 - 10k (I_t + I_c) \]
\[ = 10 - 10k (1.316 \text{mA} + 1.582 \text{mA}) \]
\[ = 4.18 \geq V_{CE} (sat) \]

\[ \beta = 550 \]
Example: Find $\Phi$

\[-10 + (\beta I_b + I_2) 10k + I_2 \times 100k \times 7 + (\beta + 1) I_b \times 1k = 0\]

\[\Rightarrow I_2 = I_b + I_1\]

we need to find $I_1$

\[-68k \times I_1 + 7 + (\beta + 1) I_b \times 1k = 0\]

\[I_1 = \frac{7 + (\beta + 1) I_b \times 1k}{68k}\]

\[-10 + 50 \times I_b \times 10k + 110k \left( \frac{I_b + 157 + \beta I_b \times 1k}{68k} \right)\]

\[
\begin{align*}
I_b &= 1.1009 \times 10^{-5} \\
I_C &= 1.55 mA \\
I_1 &= 1.018 mA, \ I_2 = 1.029 mA
\end{align*}
\]

\[V_{CE} = 10 - 10k (1.55 mA + 1.029 mA) - 51 \times 1.1009 \times 10^{-6} \times 1k\]

\[= 3.639.
\]
Example: find Q point

Assume active

\[ \text{voltage divider circuit} \]

\[ \beta \geq 10 \quad \Rightarrow \quad 99 \times 4.05k \geq 470 \times 10 \]

Solve by approximation method.

\[ V_b = \frac{15 \times 470}{800} = 8.81 \]

\[ V_{be} = 1.7 \quad \Rightarrow \quad V_C = V_b - 1.7 = 8.11 \]

\[ I_E = \frac{8.11}{4.05k} = 2m \approx I_C \]

\[ V_{CE} = 15 - 2m(10k + 4.05k) = -13.14 \quad \Rightarrow \quad \text{Our assumption is wrong the transistor is saturation} \]

Resolve

Assume saturation.

\[ V_{CE} = V_{CE(sat)} = 12 \quad \text{or} \quad V_{CE(sat)} = 0 \]

\[ I_C = \frac{15 - V_{CE(sat)}}{10k + 4.05k} = \frac{15}{10.05} = 1.49m \quad \Rightarrow \quad \text{Sat} \]

\[ 10 \]
Example: (pnp).

Check:

\[ \beta_{RE} > 10k \Rightarrow 9.5 \times 2k > 10 \times 10k \]

\[ V_B = \frac{10 \times 40k}{50k} = 8 \]

\[ V_E = 8.7 \]

\[ I_E = \frac{10.7 - 8.7}{2k} = 1m \]

\[ V_{CE} = 10.7 - 6k \times 1m = 4.7 > V_{CE} (sat) \]