Chapter 8: FET Amplifiers
Introduction

FETs provide:

- Excellent voltage gain
- High input impedance
- Low-power consumption
- Good frequency range
FET Small-Signal Model

**Transconductance**

The relationship of a change in $I_D$ to the corresponding change in $V_{GS}$ is called *transconductance*. Transconductance is denoted $g_m$ and given by:

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$
Graphical Determination of $g_m$

\[ g_m = \frac{\Delta I_D}{\Delta V_{GS}} \quad (= \text{Slope at } Q\text{-point}) \]

Diagram showing the graphical determination of $g_m$ with points $V_P$, $I_D$, $I_{DSS}$, and $Q$-Point.
Mathematical Definitions of $g_m$

\[
g_m = \frac{\Delta I_D}{\Delta V_{GS}}
\]

\[
g_m = \frac{2I_{DSS}}{|V_P|} \left[ 1 - \frac{V_{GS}}{V_P} \right]
\]

Where $V_{GS} = 0$V

\[
g_{m0} = \frac{2I_{DSS}}{|V_P|}
\]

\[
g_m = g_{m0} \left[ 1 - \frac{V_{GS}}{V_P} \right]
\]

Where \( 1 - \frac{V_{GS}}{V_P} = \sqrt{\frac{I_D}{I_{DSS}}} \)

\[
g_m = g_{m0} \left( 1 - \frac{V_{GS}}{V_P} \right) = g_{m0} \sqrt{\frac{I_D}{I_{DSS}}}
\]
FET Impedance

Input impedance:

\[ Z_i = \infty \Omega \]

Output Impedance:

\[ Z_o = r_d = \frac{1}{y_{os}} \]

where:

\[ r_d = \frac{\Delta V_{DS}}{\Delta I_D} \bigg|_{V_{GS} = \text{constant}} \]

\[ y_{os} = \text{admittance parameter listed on FET specification sheets.} \]
FET AC Equivalent Circuit
Common-Source (CS) Fixed-Bias Circuit

The input is on the gate and the output is on the drain.

There is a 180° phase shift between input and output.
Calculations

Input impedance:

\[ Z_i = R_G \]

Output impedance:

\[ Z_o = R_D \parallel r_d \]

\[ Z_o \approx R_D \quad \text{if} \quad r_d \geq 10R_D \]

Voltage gain:

\[ A_v = \frac{V_o}{V_i} = -g_m (r_d \parallel R_D) \]

\[ A_v = \frac{V_o}{V_i} = -g_m R_D \quad \text{if} \quad r_d \geq 10R_D \]
Common-Source (CS) Self-Bias Circuit

This is a common-source amplifier configuration, so the input is on the gate and the output is on the drain.

There is a 180° phase shift between input and output.
Calculations

**Input impedance:**

\[ Z_i = R_G \]

**Output impedance:**

\[ Z_o = r_d \parallel R_D \]
\[ Z_o \approx R_D \quad \text{if } r_d \geq 10R_D \]

**Voltage gain:**

\[ A_v = -g_m (r_d \parallel R_D) \]
\[ A_v = -g_m R_D \quad \text{if } r_d \geq 10R_D \]
Common-Source (CS) Self-Bias Circuit

Removing $C_s$ affects the gain of the circuit.
Calculations

Input impedance:

\[ Z_i = R_G \]

Output impedance:

\[ Z_o \approx R_D \quad | \quad r_d \geq 10R_D \]

Voltage gain:

\[ A_V = \frac{V_o}{V_i} = -\frac{g_m R_D}{1 + g_m R_S + \frac{R_D + R_S}{r_d}} \]

\[ A_V = \frac{V_o}{V_i} = -\frac{g_m R_D}{1 + g_m R_S} \quad | \quad r_d \geq 10(R_D + R_S) \]
Common-Source (CS) Voltage-Divider Bias

This is a common-source amplifier configuration, so the input is on the gate and the output is on the drain.
Impedances

Input impedance:

\[ Z_i = R_1 \parallel R_2 \]

Output impedance:

\[ Z_o = r_d \parallel R_D \]

\[ Z_o \approx R_D \quad r_d \geq 10R_D \]

Voltage gain:

\[ A_v = -g_m \left( r_d \parallel R_D \right) \]

\[ A_v = -g_m R_D \quad r_d \geq 10R_D \]
Source Follower (Common-Drain) Circuit

In a common-drain amplifier configuration, the input is on the gate, but the output is from the source.

There is no phase shift between input and output.
Impedances

**Input impedance:**

\[ Z_i = R_G \]

**Output impedance:**

\[ Z_o = r_d \parallel R_S \parallel \left| \frac{1}{g_m} \right| \]

\[ Z_o \cong R_S \parallel \left| \frac{1}{g_m} \right| r_d \geq 10R_S \]

**Voltage gain:**

\[ A_v = \frac{V_o}{V_i} = \frac{g_m (r_d \parallel R_S)}{1 + g_m (r_d \parallel R_S)} \]

\[ A_v = \frac{V_o}{V_i} = \frac{g_m R_S}{1 + g_m R_S} \quad r_d \geq 10 \]
Common-Gate (CG) Circuit

The input is on the source and the output is on the drain.

There is no phase shift between input and output.
Calculations

Input impedance:

\[ Z_i = R_S \parallel \left[ \frac{r_d + R_D}{1 + g_m r_d} \right] \]

\[ Z_i \cong R_S \parallel \frac{1}{g_m} r_d \geq 10R_D \]

Output impedance:

\[ Z_o = R_D \parallel r_d \]

\[ Z_o \cong R_D \bigg| r_d \geq 10 \]

Voltage gain:

\[ A_v = \frac{V_o}{V_i} = \left[ g_m R_D + \frac{R_D}{r_d} \right] \left[ 1 + \frac{R_D}{r_d} \right] \]

\[ A_v = g_m R_D \bigg| r_d \geq 10R_D \]
D-Type MOSFET AC Equivalent
E-Type MOSFET AC Equivalent

$g_m$ and $r_d$ can be found in the specification sheet for the FET.

$g_m = |y_{fs}|$, $r_d = \frac{1}{|y_{os}|}$
Common-Source Drain-Feedback

There is a 180° phase shift between input and output.
Calculations

**Input impedance:**

\[
Z_i = \frac{R_F + r_d \parallel R_D}{1 + g_m (r_d \parallel R_D)}
\]

\[
Z_i \approx \frac{R_F}{1 + g_m R_D} \quad R_F >> r_d \parallel R_D, r_d \geq 10R_D
\]

**Output impedance:**

\[
Z_o = R_F \parallel r_d \parallel R_D
\]

\[
Z_o \approx R_D \quad R_F >> r_d \parallel R_D, r_d \geq 10R_D
\]

**Voltage gain:**

\[
A_v = -g_m (R_F \parallel r_d \parallel R_D)
\]

\[
A_v \approx -g_m R_D \quad R_F >> r_d \parallel R_D, r_d \geq 10R_D
\]
Common-Source Voltage-Divider Bias
**Calculations**

**Input impedance:**

\[ Z_i = R_1 \parallel R_2 \]

**Output impedance:**

\[ Z_o = r_d \parallel R_D \]
\[ Z_o \cong R_D \mid r_d \geq 10 \]

**Voltage gain:**

\[ A_v = -g_m \left( r_d \parallel R_D \right) \]
\[ A_v \cong -g_m R_D \mid r_d \geq 10R_D \]
Summary Table
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Fixed-bias
[JFET or D-MOSFET]

Self-bias
Unbypassed $R_S$
[JFET or D-MOSFET]

Self-bias
bypassed $R_S$
[JFET or D-MOSFET]

Voltage-divider bias
[JFET or D-MOSFET]
Troubleshooting

Check the DC bias voltages:

If not correct check power supply, resistors, FET. Also check to ensure that the coupling capacitor between amplifier stages is OK.

Check the AC voltages:

If not correct check FET, capacitors and the loading effect of the next stage.
Practical Applications

Three-Channel Audio Mixer
Silent Switching
Phase Shift Networks
Motion Detection System