ECOM5335 – VLSI Design

Final Project Requirements Sheet

This document gives you enough information to get started on your final project for the course. If you need any additional information, you have to check with the instructor.

The purpose of the project is to apply the concepts of the course and come up with a complete VLSI design.

A complete VLSI design includes:

- Logic design (gate level) (1 point)
- Circuit design (transistor level) (1 point)
- Simulation using H-Spice to verify functionality and match results with specifications. (6 points)
- Layout the design and simulate to verify functionality. (3 points)

Deliverables:

- Specification sheet (project idea). **Due on November 28th.** (1 point)
- A complete report that covers all the design process steps. **Due on December 17th** (5 points)
- Complete spice netlists and simulation results (waveforms and measurements) to be included in the report. **Due on December 10th.**
- In class presentation (5-10 minutes) that highlights the main points in your design. **Due on the week of December 17th**. (3 points)

You can either choose a project idea from the provided list, or bring your own idea. You can work on the project in a group of 2 students for male students and 2-3 students per group for female students.

Proposed Project Ideas

1) 3 Inputs LUT (preferred)
    a. Using pass gates without buffers.
    b. Using pass gates with buffers.
    c. Using logic gates.
2) Clock Divider with select line.
3) Counter:
    a. Binary
    b. Grey
    c. One hot
    d. …
4) Multiplier 4bit x 4bit w/pipeline. Compare to without pipeline.
5) Carry look ahead adder.
6) If you another project idea, you can submit it, but you have to get the ok before you start.

I will not accept having many groups working on one project idea. So try to work on a different idea than others. If only few project ideas were chosen, I will reassign the ideas myself.