Experiment 4

RESISTOR-TRANSISTOR LOGIC (RTL) GATES

Objectives

- Be familiar with logic gates using resistors and bipolar transistor connected with RLT techniques.
- Studying the internal connection of AND, OR, NAND, and NOR.
- To determine the VTC of these gates.

Equipments

- Resistors – TR(2N2222)
- Voltmeter
- Power supply
- Orcad software program

Introduction

The logic family presented in this experiment is Resistor-Transistor logic (RTL). As the name implies, circuits of the Resistor-Transistor logic family are constructed from resistors and transistors (BJTs). RTL was the first logic family to become commercially available. Inverters (NOT), non inverters (buffers), AND, OR, NAND, and NOR gates can all be constructed with RTL logic. In addition, low, medium, and high power versions of the various RTL gates were obtained by varying the magnitudes of the resistors. Large resistors are used for low power applications and small resistors are used for high power applications.

Theoretical background

- 2-Input NOR gate
  
  NOR gates are commonly used in integrated circuits because of the simple circuits that implement their function. Other types of gates can be built using combination of NOR gates, the NOR is a (functionally complete set).
For this circuit, the current through the single collector resistor is the sum of the BJTs and is given by

\[ I_c = \sum I_{C_i} \]

The output voltage is then

\[ V_{out} = V_{cc} - I_c R_1 \]

If all inputs are less than \( V_{BE}(FA) \) then all BJTs are cutoff. As a result, \( I_c = 0 \) and the output voltage is

\[ V_{OH} = V_{CC} \]

If any input is greater than or equal to \( V_{BE}(FA) \), the corresponding BJT conduct and if any input reaches \( V_{IH} \) the output drops to

\[ V_{OL} = V_{CE(SAT)} \]

**2-Input OR gate**

By inverting the NOR gate by using simple transistor as an inverter we may have a simple OR RTL gate.
There is another configuration that implies the same output of previous circuit

If any input is greater than or equal to $V_{BE}(FA)$, the corresponding BJT conduct and the output voltage is

$$V_{OUT} = I_e R_e$$

if any input reaches $V_{IH}$ the output is

$$V_{OH} = V_{CC} - V_{CE(SAT)}$$

And if all inputs are low, the transistors are cutoff and the output voltage is

$$V_{OL} = 0$$

**2-Input NAND gate**

A very common NAND logic is the RTL series. The main advantage of such system is the pull down network.
If all inputs are greater than or equal $V_{BE}(FA)$ then all BJTs conduct and the output voltage is

$$V_{OUT} = V_{CC} - I_c R_C$$

If any input is low, the corresponding transistor is cutoff and the output voltage is

$$V_{OH} = V_{CC}$$

If all inputs reach $V_{IH}$ the output is

$$V_{OL} = 2 * V_{CE\,(SAT)}$$

❖ **2-Input AND gate**

By inverting the NAND gate by using simple transistor as an inverter we may have a simple AND RTL gate.

![Figure 5](image)

There is another configuration that implies the same output of previous circuit

![Figure 6](image)
If all inputs are greater than or equal $V_{BE(FA)}$ then all BJTs conduct and the output voltage is

$$V_{OUT} = I_c R_e$$

If all inputs reach VIH the output is

$$V_{OH} = V_{CC} - 2 \cdot V_{CE(SAT)}$$

And if any input is low, the corresponding transistor is cutoff and the output voltage is

$$V_{OL} = 0$$

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**Procedures:**

**Part 1:**

1. Construct the circuit shown in Figure 1, $V = 5V$, $R1 = 1K$, $R2 = 10K$
2. find the truth table filling the following

<table>
<thead>
<tr>
<th>$V_A$</th>
<th>$V_B$</th>
<th>$V_{OUT}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>5</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>5</td>
<td></td>
</tr>
</tbody>
</table>

3. Draw the VTC of this gate by making $V_A = V_B = V_{IN}$ and filling the following table:

<table>
<thead>
<tr>
<th>$V_{IN}$</th>
<th>0</th>
<th>0.1</th>
<th>0.2</th>
<th>0.3</th>
<th>0.4</th>
<th>0.5</th>
<th>0.6</th>
<th>0.7</th>
<th>0.8</th>
<th>0.9</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{OUT}$</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

4. Determine $V_{OH}, V_{OL}, V_{IH}, V_{IL}$

**Part 2:**

1. Draw the circuits shown in Figure 2 & Figure 3 by using the Orcad and show the results.

$V = 5V$, $R1 = 1K$, $R2 = RE = 10K$
Part 3:

1. Construct the circuit shown in Figure 4, \( V = 5V, R_1 = 1K, R_2 = 10K \)
2. find the truth table filling the following

<table>
<thead>
<tr>
<th>( V_A )</th>
<th>( V_B )</th>
<th>( V_{OUT} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>5</td>
<td>0</td>
<td>5</td>
</tr>
<tr>
<td>5</td>
<td>5</td>
<td>5</td>
</tr>
</tbody>
</table>

3. Draw the VTC of this gate by making \( V_A = V_B = V_{IN} \) and filling the following table:

<table>
<thead>
<tr>
<th>Vin</th>
<th>0</th>
<th>0.1</th>
<th>0.2</th>
<th>0.3</th>
<th>0.4</th>
<th>0.5</th>
<th>0.6</th>
<th>0.7</th>
<th>0.8</th>
<th>0.9</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vout</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
</tr>
</tbody>
</table>

4. Determine \( V_{OH}, V_{OL}, V_{IH}, V_{IL} \)

Part 4:

1. Draw the circuits shown in Figure 5 && Figure 6 by using the Orcad and show the results.

\[ V = 5V, R_1 = 1K, R_2 = R_E = 10K \]