Digital System Design

Homework Policy:

- Groups are allowed up to 2.
- One can share the ideas with her colleges, but copied Hws lead to ZERO grade.
- Homework has to be formally printed. (Handwritten is not allowed).
- Submission will be on Sat. 22.09.2012 until 15:00.

Exercise 1 (Concepts) [Points: 3]
Briefly outline the purposes of the following VHDL modelling constructs: entity declaration, behavioural architecture body, structural architecture body, process statement, signal assignment statement and port map.

Exercise 2 (Design-behavioural) [Points: 5]
Write an entity declaration and a behavioural architecture body for a two-input multiplexer, with input ports $a$, $b$ and $sel$ and an output port $z$. If the $sel$ input is 0, the value of $a$ should be copied to $z$, otherwise the value of $b$ should be copied to $z$. Write a test bench for the multiplexer model, and test it using a VHDL simulator.

Exercise 3 (Design-structural) [Points: 5]
Write an entity declaration and a structural architecture body for a 4-bit-wide multiplexer, using instances of the 2-bit multiplexer from previous exercise. The input ports are $a_0$, $a_1$, $a_2$, $a_3$, $b_0$, $b_1$, $b_2$, $b_3$ and $sel$, and the output ports are $z_0$, $z_1$, $z_2$ and $z_3$. When $sel$ is 0, the inputs $a_0$ to $a_3$ are copied to the outputs, otherwise the inputs $b_0$ to $b_3$ are copied to the outputs. Write a test bench for the multiplexer model, and test it using a VHDL simulator.

Exercise 4 (VHDL) [Points: 2]
Why does one use VHDL instead of higher programming language C++, Java....etc? In other words, what is the purpose of VHDL?