Homework Policy:
- Groups are allowed up to 2.
- One can share the ideas with her colleges, but copied Hws lead to ZERO grade.
- Homework has to be formally printed. (Handwritten is not allowed).
- Submission will be on Sat. 19.11.2012 until 15:00.

Exercise 1

The NOT operator allows the inversion of binary values. For example, if \( x = \text{"1000"} \) is a \text{STD_LOGIC_VECTOR} value, then \( \text{NOT } x \) could be used, producing \( \text{"0111"} \). However, if \( x \) had been declared as an \text{INTEGER}, such operation would not be allowed. Write a “not” function capable of inverting integers. (Suggestion: See section 4.4 and example 11.6.)

Exercise 2:

A) You are to design a “Serial Sequence Detector”. Your design will take in a clock, reset, and a one-bit data signal. Your design will check the input data signal on the rising edge of the input clock. When it finds the sequence “01100110”, it will assert an output signal “Found” for one clock cycle.
Exercise 3:

Wire VHDL code that describe this FSM design