Problem 1: State weather the following is True or False and CORRECT THE MISTAKE (5 points).

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>T</td>
<td>Memory is a key bottleneck in many embedded systems.</td>
</tr>
<tr>
<td>F</td>
<td>Using Loop splitting techniques will increase decrease the amount of energy consumed in the CPU core.</td>
</tr>
<tr>
<td>F</td>
<td>In memory management, static and dynamic buffer management techniques are is preferable.</td>
</tr>
<tr>
<td>T</td>
<td>The SC140 processor is organized into two clusters that perform different functions.</td>
</tr>
<tr>
<td>T</td>
<td>Limited or irregular processor resources are influential when operations are performed.</td>
</tr>
<tr>
<td>F</td>
<td>A general purpose uProcessor hasn’t an on chip ROM.</td>
</tr>
<tr>
<td>F</td>
<td>Most instructions in CISC are executed in one or two cycles. Takes many cycle</td>
</tr>
<tr>
<td>F</td>
<td>We cannot move literal values directly into the general purpose RAM location in the PIC18.</td>
</tr>
<tr>
<td>F</td>
<td>In PIC18, the CPU can fetch two one byte instructions in each clock cycle.</td>
</tr>
<tr>
<td>F</td>
<td>The function of each SFR cannot be changed. (is fixed by the CPU designer at the time of design)</td>
</tr>
</tbody>
</table>

Problem 2: Choose the best answer (6 points).

What is the status of the C and Z flag after the following Code?

```
MOVLW 0h
ADDLW 9E
ADDLE 62
```

- C=1 and Z= 0
- C=0 and Z= 0
- C=0 and Z= 1

For the next table, where data are shown in hexadecimal, What is the value of WREG after executing the following instructions?

<table>
<thead>
<tr>
<th>Address Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>026H 22</td>
</tr>
<tr>
<td>028H 13</td>
</tr>
<tr>
<td>030H 1A</td>
</tr>
<tr>
<td>032H 20</td>
</tr>
<tr>
<td>034H 00</td>
</tr>
</tbody>
</table>

A.  
```
MOVLW 0A0h
MOVF 0x30, W
```

- 1A
- AA
- 0A

B.  
```
ADDWF 0x28H, W
```

- 0x00
- 0x2D
- 0x13
- 0x28

C.  
To move the value 20 from the location 0x32h to 0x26h, we use the following instruction

- MOVFF 0x26, 0x32
- MOVFF 0x32, 0x26
COPY 0x32, 0x26

MOVF 0x26, 0x32

PIC18C1023 has _______KB of code memory.

4
2
1
0

For the input file picTest.o, the Linker outs the following files except
picTest.hex
picTest.map
picTest.lst
picTest.cod
picTest.err

The status register is a(n) ________-bit register
21
8
16
1
5

Which of the following instruction is legal?
ADDLW 5AH
ADDLW $500
ADDLW 'A'
ADDLW .300
ADDLW b'00000102'

Problem 3: Answer the following Questions. (6 points)

1. Which is better Assembly language or C language?
Both of them has its advantage and disadvantages.

2. What are the essential properties of a Petri net?
The structure of the Petri net is defined by the places, the transitions, and the arcs. One or more tokens move around the Petri net as the system state changes. Firing rules at the transitions govern how tokens move.

3. For the CPUs architecture,
   a) What is the difference between DSP Processor and VLIW?
   b) What does VLIW stand for?
   c) How many instructions can the VLIW execute at maximum?

   a)
   b) Very large Instruction Word.
   c) 5 instructions.

Problem 4: Embedded System Design. (10 points)

A small sensor is used to monitor some falcons in their environments. For the designed sensor, the scientists want to have one input X and one output Z such that Z is 1 if the last two inputs are different and 0 if the last two inputs are the same. For example, if the inputs are 0010010011 then the outputs would be 0011011010. The output will be sent via external wireless model.
Assume that there is one input per clock cycle.

   a) What are the functional requirements and non-functional requirements for the system?

   ……………………………………………………………………………………………………………………………
b) Draw a state diagram for your finite state machine. (state its type)

Moore state machine solution

Mealy state machine solution

Either a Moore or Mealy solution is acceptable.

c) If your sensor is part of a sensor network, mention two attacks that may attack your system.
1. Physical layer: jamming, tampering.
2. Link layer: collision, exhaustion, unfairness.
4. Transport layer: flooding, de-synchronization.

d) Suppose you write 1824 byte of code, and suppose that you want to collect 100-byte of data and send them, which of the following PICs you choose for your design and why? (choose only and only one)

<table>
<thead>
<tr>
<th>PIC</th>
<th>I/O Pins</th>
<th>GPR</th>
<th>Price</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>PIC12F508</td>
<td>5</td>
<td>25</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>PIC16F84</td>
<td>13</td>
<td>68</td>
<td>3</td>
<td></td>
</tr>
<tr>
<td>PIC18F1220</td>
<td>16</td>
<td>256</td>
<td>5</td>
<td>Not Available</td>
</tr>
<tr>
<td>PIC18F452</td>
<td>34</td>
<td>1536</td>
<td>10</td>
<td></td>
</tr>
<tr>
<td>PIC18F2220</td>
<td>25</td>
<td>512</td>
<td>5</td>
<td></td>
</tr>
<tr>
<td>PIC18F458</td>
<td>32</td>
<td>1536</td>
<td>10</td>
<td></td>
</tr>
<tr>
<td>PIC18F8722</td>
<td>70</td>
<td>3938</td>
<td>25</td>
<td></td>
</tr>
<tr>
<td>PIC18F4550</td>
<td>36</td>
<td>1888</td>
<td>12</td>
<td>Not Available</td>
</tr>
</tbody>
</table>

RAM should be greater than 100 Bytes
ROM should be greater than 1824 Bytes
The best one is PIC18F2220 since it is the cheapest one.
Problem 5: Scheduling and Register Allocation. (8 points)

(a) Draw the Variable Lifetime Graph.

<table>
<thead>
<tr>
<th>cycle</th>
<th>U1</th>
<th>U2</th>
<th>U3</th>
<th>U4</th>
<th>U5</th>
<th>U6</th>
</tr>
</thead>
<tbody>
<tr>
<td>C0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>C1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>C2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Inputs: v1, v2, v3, v4
Outputs: u5, u6
op1: u1 <-- v1 + v2
op2: u2 <-- v3 - v2
op3: u3 <-- v3 + v4
op4: u4 <-- u1 - u2
op5: u5 <-- u2 + u3
op6: u6 <-- u4 - u3

(b) How many Registers are required to store the six output variable?

3 registers

(c) Draw the Variable to Register allocation (this means, How are the instruction scheduled).

(d) Assume that you have one adder and one subtracter, what is the minimum number of registers? Draw the Variable to register allocation.