Experiment Objectives:
1. To understand the operation theory of FSK demodulator.
2. To implement the FSK detector circuit by using PLL.
3. To understand the operation theory of comparator by using operational amplifier as voltage level converter.

Experiment theory:

In experiment 7 we use FSK modulator for long distance communication, which the voltage level of digital signal has been converted to frequency. Therefore, at the receiver, we have to recover the FSK signal to digital signal, that means the frequency should be converted back to voltage. We use phase locked loop (PLL) as FSK demodulator. PLL is a kind of automatic tracking system, which is able to detect the input signal frequency and phase. PLL is widely used in wireless applications, such as AM demodulator, FM demodulator, frequency selector and so on. In the digital communications, various types of digital PLLs are developed. Digital PLL is very useful in carrier synchronization, bit synchronization and digital demodulation.

1. Asynchronous FSK detector:

The block diagram of asynchronous FSK detector is shown in figure 8.1. In figure 8.1, we can see that at the receiver parts, there are two low-pass filters, which their center frequencies are $\omega_c + \omega_D$ and $\omega_c - \omega_D$, respectively. By using the characteristic of the filter, we can obtain the $\omega_c + \omega_D$ (Digital signal represents as 1) and $\omega_c - \omega_D$ (Digital signal represents as 0). Then combine the digital signal after demodulation, finally, the original digital signal can be obtain at the output terminal. Since the fixed frequency deviation of the carrier signal ($\omega_c$) is quite small, therefore, the usage of sharp filter is its disadvantage.

Figure 8.1 Block diagram of asynchronous FSK detector.
2. Synchronous FSK detector:

Let the received data signal $V_{\text{FSK}}(t)$ multiply by a local oscillation (LO) signals $\cos(\omega_c+\omega_D)t$ or $\cos(\omega_c-\omega_D)t$ as shown in equations (8.1) and (8.3). Then we can obtain $\cos[2(\omega_c+\omega_D)]t$, which the digital signal frequency is represented as 1 or $\cos[2(\omega_c-\omega_D)]t$, which the digital signal frequency is represented as 0. After that by using the filter to remove the second order harmonics and DC voltage, then we can obtain the original digital signal as shown in figure 8.2.

In this section, we utilize the theory of mathematic to solve the FSK demodulation as shown in equation (8.1). The synchronous FSK detector needs two LO oscillators, which the LO frequencies are $\omega_c-\omega_D$ and $\omega_c+\omega_D$, respectively, as shown in figure 8.2. When the received signal is $A\cos(\omega_c+\omega_D)t$, then we get:

$$v(t) = A\cos(\omega_c+\omega_D)t \left[ \cos(\omega_c+\omega_D)t - \cos(\omega_c-\omega_D)t \right]$$

$$= A\cos^2(\omega_c+\omega_D)t - A\cos(\omega_c+\omega_D)t \cos(\omega_c-\omega_D)t$$

$$= \frac{A}{2} - \frac{A}{2} \left[ \cos(2\omega_ct) + \cos(2\omegaDt) - \cos(2\omega_c t + \omega_D t) \right] \text{ .......................................................... 8.1}$$

By using a filter to remove all the unwanted signal in equation (8.1), then the represented output signal is 1 and we can rewritten equation (8.1) as follow:

$$v_1(t) = \frac{A}{2} \cos[2(\omega_c + \omega_D)t] \text{ .................................................. 8.2}$$

Where:
- $\omega_c$: carrier frequency.
- $\omega_D$: Signal frequency.

When the received signal is $A\cos(\omega_c-\omega_D)t$, then we get:

$$v(t) = A\cos(\omega_c-\omega_D)t \left[ \cos(\omega_c+\omega_D)t - \cos(\omega_c-\omega_D)t \right]$$

$$= -A\cos^2(\omega_c-\omega_D)t + A\cos(\omega_c+\omega_D)t \cos(\omega_c-\omega_D)t$$

$$= -\frac{A}{2} - \frac{A}{2} \left[ \cos(2\omega_c t - \omega_D t) - \cos(2\omega_c t) - \cos(2\omega_D t) \right] \text{ .......................................................... 8.3}$$

By using a filter to remove all the unwanted signal in equation (8.3), then the represented output signal is 0 and we can rewritten equation (8.1) as follow:

$$v_2(t) = -\frac{A}{2} \cos[2(\omega_c - \omega_D)t] \text{ .................................................. 8.4}$$
Generally, phase locked loop (PLL) can be divided into 3 main parts, which are the phase detector (PD), loop filter (LF) and voltage controlled oscillator (VCO). The block diagram of PLL is shown in figure 8.3.

In figure 8.3, when the input signal frequency changes, the output signal of the phase detector will change and so as well as the output voltage. We can use this characteristics to design the FSK demodulator. Let the FSK signal frequencies as $f_1$ and $f_2$, then these signals are inputted to the input terminal of figure 8.3. When the input signal frequency is $f_1$, the output voltage will be $V_1$. When the input signal frequency is $f_2$, the output voltage is $V_2$. At this moment, we have converted the frequency to voltage. If we add a comparator at the output terminal of PLL, the reference voltage will lie between $V_1$ and $V_2$, then at the output terminal of comparator, we are able to obtain the digital signal, which is the demodulated FSK signal.

![Figure 8.2 Block diagram of synchronous FSK detector.](image1)

In this experiment, we implement the FSK demodulator by using LM565 PLL as shown in figure 8.4. The operation frequency of LM565 PLL is below 500 kHz and the internal circuit diagram is shown in figure 8.4. It includes phase detector, voltage controlled oscillator and amplifier. The phase detector is a double-balanced modulator type circuit and the VCO is integrated Schmitt circuit.

![Figure 8.3 Block diagram of PLL](image2)
Pin 1 is connected to negative voltage supply, -5 V. Pins 2 and 3 are connected to the input signals, but normally pin 3 will connect to ground. If pins 4 and 5 are connected to frequency multiplier, then various multiplications of frequencies can be obtained. In this experiment, we need not use the frequency multiplier; therefore, these two pins are shorted. Pin 6 is the reference voltage output. The internal resistor (R_x) of pin 7 and the external capacitor (C_3) comprise a loop filter. Pin 8 is connected to timing resistor (VR_1). Pin 9 is connected to timing capacitor (C_2). Pin 10 the positive voltage supply +5 V of LM565. The important parameters of LM565 PLL circuit design are as follow:

1) The free-Running Frequency of LM565

When LM565 without any input signal, the output signal of VCO is called free-running frequency. The C_2 is timing capacitor and the variable resistor VR_1 is timing resistor. The freerunning frequency (f_o) of VCO of the LM565 is determined by C_2 and VR_1. The expression is:

\[ f_o \approx \frac{1.2}{4VR_1C_2} \]

2) The locked Range of LM565

When the PLL is in locked condition, if the frequency of the input signal (f_i) deviates from f_o, then the PLL will remain in the locked condition. When f_i reaches a certain frequency, which the PLL is not able to lock, then the difference between f_i and f_o is called the locked range.

The locked range of LM565 can be expressed as:

\[ f_L = \frac{8f_o}{V_c} = \frac{8f_o}{V_{CC} - V_{EE}} \]
3) The Capture Range of LM565

The initial mode of PLL is in unlocked condition, then the frequency of the input signal \( f_i \) will come near to \( f_o \). When \( f_i \) reaches a certain frequency, the PLL will be in locked condition. At this moment, the difference between \( f_i \) and \( f_o \) is called the capture range. The captured range of LM565 can be expressed as:

\[
f_c = \frac{1}{2\pi} \sqrt{\frac{2\pi f_L}{3.6 \times 10^5 \times C_2}}
\]

In figure 8.4, pin 7 of LM565 is connected to \( R_3 \), \( R_4 \), \( R_5 \), \( C_3 \), \( C_4 \) and \( C_5 \) to comprise a low-pass filter. The objective is to remove the unwanted signal, which will cause the comparator produce incorrect action. \( \mu A741 \) is the comparator and its reference voltage is inputted at pin 6 of LM565. The output voltage of LM565 will pass through \( \mu A741 \) and \( D_1 \) to obtain the output voltage of digital signal of TTL level.
Experiment items:

Experiment 1: XR2206 FSK demodulator

1. Refer to the circuit diagram in figure 8.4 or figure DCS 14.1 on ETEK DCS-6000-07 module. Without adding any signal at the input terminal (FSK I/P), then by using oscilloscope, observe on the VCO output (TP1) of LM565, adjust variable resistor VR₁ so that the free-running frequency of LM565 operates at 1170 Hz.

2. At the input terminal (FSK I/P) of figure DCS 14.1, input 4 V amplitude and 870 Hz sine wave frequency. By using oscilloscope and switching to DC channel, then observe on the output signal waveform of FSK I/P, TP1, charge and discharge test point (TP2), low-pass loop circuit 1 (TP3), low-pass loop circuit 2 (TP4), low-pass loop circuit 3 (TP5), low-pass loop circuit 4 (TP6), reference voltage of the comparator (TP7), output terminal of the comparator (TP8) and data signal output port (Data O/P). Finally, record the measured results in table 8.1.

3. At the input terminal (FSK I/P) of figure DCS 14.1, input 4 V amplitude and 1370 Hz sine wave frequency. Repeat step 2 and record the measured results in table 8.2.

4. Refer to figure 7.3 with R₁= 7.5 kΩ and R₅= 15 kΩ or refer to figure DCS 13.1 on ETEK DCS-6000-07 module. Let J2 and J4 be open circuit, J3 and J5 be short circuit.

5. At the data signal input terminal (Data I/P), of figure DCS 13.1, input 5 V amplitude, 150 Hz TTL signal.

6. Connect the modulated FSK signal (FSK O/P) of figure DCS 13.1 to the input terminal (FSK I/P) of figure DCS 14.1. By using oscilloscope, observe on the output signal waveform of TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8 and Data O/P. Finally, record the measured results in table 8.3.

7. According to the input signal in table 8.3, repeat step 5 to step 6 and record the measured results in table 8.3.
Experiment 2: LM566 FSK demodulator

1. Refer to the circuit diagram in figure 7.6 or figure DCS13.2 on ETEK DCS-6000-07 module.

2. From figure DCS13.2, let the two terminal of I/P be short circuit and J1 be open circuit, i.e. at the data signal input terminal (Data I/P), input 0 V DC voltage. By using oscilloscope, observe on the output signal waveform of the VCO output port (TP1) of LM566. Slightly adjust VR1 so that the frequency of TP1 is 1370 Hz. Again let the data signal input terminal (Data I/P) be open circuit and J1 be short circuit, i.e. input 5 V DC voltage to the data signal input terminal (Data I/P). By using oscilloscope, observe on the output signal waveform of the VCO output port (TP1) of LM566. Slightly adjust VR1 so that the frequency of TP1 is 870 Hz.

3. At the data signal input terminal (Data I/P), of figure DCS13.2, input 5 V amplitude, 150 Hz TTL signal. Connect the modulated FSK signal (FSK O/P) of figure DCS13.2 to the input terminal (FSK I/P) of figure DCS14.1. By using oscilloscope, and switching to DC channel, observe on the output signal waveform of TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8 and Data O/P. Finally, record the measured results in table 8.4.

4. According to the input signal in table 8.4, repeat step 3 and record the measured results in table 8.4.
**Measured results:**

**Table 8-1** Measured results of FSK demodulator (\(V_{in}=4V\))

<table>
<thead>
<tr>
<th>Carrier signal frequencies</th>
<th>Output signal waveforms</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Data I/P</td>
</tr>
<tr>
<td></td>
<td>TP2</td>
</tr>
<tr>
<td></td>
<td>TP4</td>
</tr>
<tr>
<td>870 Hz</td>
<td>TP6</td>
</tr>
<tr>
<td></td>
<td>TP8</td>
</tr>
</tbody>
</table>

**NOTE:**

**Table 8-2:** Repeat table 8-1 but with carrier frequency 1370 Hz.
Table 8-3 Measured results of FSK demodulator by using 2206 IC.
(J3, J5 SC; J2, J4 OC)

<table>
<thead>
<tr>
<th>Carrier signal frequencies</th>
<th>Output signal waveforms</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data I/P</td>
<td>TP1</td>
</tr>
<tr>
<td></td>
<td>TP2</td>
</tr>
<tr>
<td></td>
<td>TP4</td>
</tr>
<tr>
<td>V_p=5V 150 Hz</td>
<td>TP6</td>
</tr>
<tr>
<td></td>
<td>TP8</td>
</tr>
</tbody>
</table>

**NOTE:**
Repeat table 8-3 with carrier frequency 200 Hz.
Table 8-4 Measured results of FSK demodulator by using LM566.

<table>
<thead>
<tr>
<th>Carrier signal frequencies</th>
<th>Output signal waveforms</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data I/P</td>
<td>TP1</td>
</tr>
<tr>
<td></td>
<td>TP2</td>
</tr>
<tr>
<td></td>
<td>TP3</td>
</tr>
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<td></td>
<td>TP4</td>
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<tr>
<td></td>
<td>TP5</td>
</tr>
<tr>
<td></td>
<td>TP6</td>
</tr>
<tr>
<td></td>
<td>TP7</td>
</tr>
<tr>
<td>V_p=5V 150 Hz</td>
<td>Data O/P</td>
</tr>
</tbody>
</table>

**NOTE:**
Repeat table 8-3 with carrier frequency 200 Hz.