Objectives:

1- To understand the operation theory of Frequency Shift Keying (FSK) modulation & demodulation.
2- To implement the BFSK modulator by VCO.
3- To implement the BFSK detector by using PLL.

Theory:

1. FSK Modulation

FSK technique is to modulate the data signal to different frequencies to achieve effective transmission. At the receiver, the data signal will be recovered based on the different frequencies of the received signal.

The general analytic expression for FSK modulation is

$$X_{FSK}(t) = \sqrt{\frac{2E}{T}} \cos(w_i t + \phi_0), \ 0 < t < T, \ i = 1, 2, 3, \ldots \ldots, M$$  \hspace{1cm} (6.1)

Where the frequency term $w_i$ has $M$ discrete values, the phase and amplitude is arbitrary constant. If we choose $M=2$, the $X_{FSK}(t)$ signal will transmit the binary signal, therefore, the values of frequencies are $F_1$ and $F_2$. When input logic is 1, then the signal’s frequency = $F_1$. When the input logic is 1, then signal’s frequency is $F_2$, so this also called Binary frequency shift keying (BFSK). Normally the difference $F_1$ and $F_2$ has to be as large as possible.
We utilize 2206IC waveform generator and LM566 “voltage controlled oscillator” to produce the modulated BFSK signal.

2. BFSK modulation by using 2206 IC

XR2206 IC is a waveform generator, which is similar to 8038 IC. Figure (2) is the circuit diagram of the FSK modulator by using 2206 IC. In figure (2), the resistor R3 and R4 comprise a voltage divided circuit. The main function of the voltage divided circuit is to let the negative voltage waveform of the 2206 IC operates normally. The oscillation frequency of XR2206 IC is determined by resistors R1&R5 and the resistor R1 located at pin 7 and the resistor R5 at pin 8. Its oscillation frequencies are

\[ f_1 = \frac{1}{2\pi R_1 C} \quad \text{and} \quad f_2 = \frac{1}{2\pi R_5 C} \]

There is an internal comparator in 2206 IC. Assume that when the input is 5 V, the output frequency is \( f_1 \), and when the input is 0 V, the output frequency is \( f_2 \). We can utilize the TTL signal at pin 9 to control the output frequency to be \( f_1 \) or \( f_2 \). Therefore, by using the characteristic of this structure, we can achieve BFSK modulation easily.

![Figure (2) The circuit diagram of the FSK modulator by using 2206 IC](image)

3. BFSK modulation by using LM566 VCO

Figure (3) is the circuit diagram of BFSK modulator using a voltage controlled oscillator (VCO), the operation theory is to convert the voltage level of data signal (TTL levels) to appropriate voltage level with specific frequency. This voltage will input to the input terminal of LM566. Then, the VCO will produce two frequencies with respect to the input voltage levels.

In this experiment, the output signal frequency of VCO is \( f_1 \) and \( f_2 \). So, we just need to adjust VR1 and VR2, the output frequencies of VCO will become \( f_1 \) and \( f_2 \) which are 1370 Hz and 870Hz.

In figure (3), the last stage is a 4th order low-pass filter to remove the unwanted signal from the VCO output.

![Figure (3) The circuit diagram of BFSK modulator using LM566 VCO](image)
4. Synchronous BFSK Demodulation

We can use Phase locked loop (PLL) to design the FSK demodulation. Generally, (PLL) can be divided into 3 mains parts which are the phase detector (PD), loop filter (LF) and voltage controlled oscillator (VCO). The block diagram of PLL is shown in figure (4).

The important parameters of LM565 PLL circuit design


When LM565 without any input signal, the output signal of VCO is called free running frequency. The $C_2$ is timing capacitor and the VR1 resistor is timing resistor. The free-running frequency ($f_0$) of VCO of LM565 is determined by $f_0 = \frac{1.2}{4 \cdot VR_1 \cdot C_2}$. 
2. The locked Range of LM565.
When the PLL is in locked condition, if the frequency of the input signal $f_i$ deviates $f_0$, then the PLL will remain in the locked condition when $f_i$ reaches a certain frequency, which the PLL is not able to lock, then the difference between $f_i$ and $f_0$ is called the locked range. $f_L = \frac{8f_0}{Vc}$

When the PLL is unlocked condition, if the frequency of the input signal $f_i$ will come near to $f_0$. When $f_i$ reaches a certain frequency, the PLL will be in locked condition, then the difference between $f_i$ and $f_0$ is called the captured range. $f_c = \frac{1}{2\pi} \sqrt{\frac{2\pi f_i}{3.6 \times 10^3 C_2}}$

Practical Parts:
1. Use DCS-6000-07 module (XR 2206 modulator) to modulate Data signal 200 Hz TTL, let J2 and J5 short circuit and J3 and J4 open circuit.
2. Use DCS-6000-07 module (LM566 modulator) to modulate Data signal 200 Hz TTL, before this let input (5V) then adjust VR1 to be the frequency of TP2 is 1370, then let input (0V) then adjust VR2 to be the frequency of TP2 is 870Hz.
3. To demodulate the modulated output signal of the first part use the synchronous demodulation.