Digital Electronics – EELE 3321

Lecture 1

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Digital Logic

- Basic Logic Gates
- Combinational Logic
- Sequential Logic
Logic Gates

NOT (Inverting-buffer)

\[ \text{out} = \text{in}' = \overline{\text{in}} \]

<table>
<thead>
<tr>
<th>In</th>
<th>Out</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

OR

\[ \text{out} = a + b \]

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>Out</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
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AND

\[ \text{out} = a \cdot b \]

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</tr>
</tbody>
</table>
Logic Gates

NOR

\[
\text{out} = \overline{a+b}
\]

\[
\begin{array}{c|c|c}
 A & B & \text{Out} \\
\hline
 0 & 0 & 1 \\
 0 & 1 & 0 \\
 1 & 0 & 0 \\
 1 & 1 & 0 \\
\end{array}
\]

NAND

\[
\text{out} = \overline{a \cdot b}
\]

\[
\begin{array}{c|c|c}
 A & B & \text{Out} \\
\hline
 0 & 0 & 1 \\
 0 & 1 & 0 \\
 1 & 0 & 0 \\
 1 & 1 & 0 \\
\end{array}
\]

Non-Inverting Buffer

[Diagrams of logic gates and non-inverting buffer]
Ideal Logic Elements

- **Ideal Static and power characteristics**
  - Operates with a single power supply ($V_{cc}$)
  - Ideal $I_{cc}$ drawn from $V_{cc}$ is zero.
  - $P_{cc} = V_{cc} \times I_{cc} = 0$ (zero power dissipation)

- $0 < V_{in} < V_{cc}/2 \rightarrow$ logical ‘0’ input
  - $\rightarrow$ gives logical ‘1’ output

- $V_{cc}/2 < V_{in} < V_{cc} \rightarrow$ logical ‘1’ input
  - $\rightarrow$ gives logical ‘0’ output

- The transition ideally occurs at $V_{cc}/2$
  - Result here is unpredictable (Avoided)
Ideal Logic Elements

- **Ideal Static and power characteristics**
  - Upon transition in the input, the output instantaneously switches to the corresponding output voltage.

- CMOS logic family is the closest logic family to meeting these ideal characteristics.

![Diagram of transient response](image)

**Transient Response**
Ideal input and output Gate Impedance

- The driving ability of the gate (Fan-out) and the transient response of the gate (gate timings) are directly dependent upon the impedance of the gate.
Ideal input and output Gate Impedance

- The driving gate must provide enough current ($I_{out}$) to drive all the load gates.

$$I_{out} = N I'_{IN}$$

When $R_{in}$ increases then $I'_{IN}$ decreases which causes $N$ to increase.

So,

$\checkmark \quad R_{in} = \infty$ is desired
**Ideal input and output Gate Impedance**

- The input Capacitance ($\dot{C}_{in}$) of the load gates must be charged through the output resistance ($R_{out}$) of the driving gate.

- We desire $R_{out} \downarrow$ to get $I_{out} \uparrow$ to charge faster $\rightarrow$ switch faster. *We ideally want $R_{out} = 0$.***

- Also $\dot{C}_{in} \downarrow$ speeds up switching (fewer load gates)
Inverter Voltage Transfer Characteristic (VTC)

- $V_{OH}$ (Output High Voltage)
- $V_{OL}$ (Output Low Voltage)
- $V_{IL}$ (Input Low): maximum input voltage that provides high out.
- $V_{IH}$ (Input High): minimum input voltage that provides low out.
- $V_M$ (Midpoint Voltage)

Logic Swing (LS):

$$V_{LS} = V_{OH} - V_{OL}$$

Transition width (TW):

$$V_{TW} = V_{IH} - V_{IL}$$
Inverter Voltage Transfer Characteristic (VTC)

$V_{OH}$, $V_{OL}$, $V_{IL}$, $V_{IH}$ are called the critical voltages of a VTC.

At $V_{M}$: $V_{IN} = V_{OUT}$

We always want,

- $V_{OH} > V_{IH}$
- $V_{OL} < V_{IL}$

Now that we have high/low, we need to consider that for Fan-out,

$$N(\text{high}) = \frac{I_{out}(\text{high})}{I'_{IN}(\text{high})}$$

$$N(\text{low}) = \frac{I_{out}(\text{low})}{I'_{IN}(\text{low})}$$

(We take the smaller of both)
Noise in Digital Circuits

- **Noise Margins**: They represent a safety margin for the high and low voltage levels. We want \( \text{NM} > \text{Actual Noise} \).

  \[
  V_{\text{NMH}} = V_{\text{OH}} - V_{\text{IH}} \\
  V_{\text{NML}} = V_{\text{IL}} - V_{\text{OL}}
  \]

- **Noise Sensitivity**: Effect of input variations

  \[
  V_{\text{NSH}} = V_{\text{OH}} - V_{\text{M}} \\
  V_{\text{NSL}} = V_{\text{M}} - V_{\text{OL}}
  \]

- **Noise Immunity**: Ability to reject noise

  \[
  V_{\text{NIH}} = V_{\text{NSH}} / V_{\text{LS}} \\
  V_{\text{NIL}} = V_{\text{NSL}} / V_{\text{LS}}
  \]
Transient Characteristics

$V_{OH}$ doesn’t necessarily reach $V_{CC}$. Similarly, $V_{IL}$ doesn’t necessarily reach 0.

- **Switching speed**
  - $t_d$: delay time
  - $t_r$: rise time
  - $t_s$: storage time
  - $t_f$: fall time
  - $t_{ON} = t_d + t_r$
  - $t_{OFF} = t_s + t_f$

$t_r$ and $t_f$ are associated with charging and discharging load capacitance
$t_d$ and $t_s$ are associated with stored charge of PN Junction
**Transient Characteristics**

- **Propagation Delay:** Time required for the output to respond to the input which is measured at the 50% point.

  - $t_{PLH}$: low-to-high propagation delay
  - $t_{PHL}$: high-to-low propagation delay

**Overall Prop. Delay:**

$$t_p(\text{avg}) = \frac{t_{PLH} + t_{PHL}}{2}$$
Power Dissipation

• Power dissipation differs depending on the state of the output, so we specify the average.

\[
P_{cc}(avg) = \frac{P_{cc}(OH) + P_{cc}(OL)}{2}
\]

\[
P_{cc}(avg) = \frac{I_{cc}(OH) + I_{cc}(OL)}{2} \frac{V_{cc}}{V_{cc}}
\]

• If we have two power supplies, then:

\[
P_{Diss}(avg) = P_{cc}(avg) + P_{EE}(avg)
\]
Both low power dissipation & short propagation delays are desirable for logic circuits

Faster propagation delay $\rightarrow$ increased power dissipation
Lower power dissipation $\rightarrow$ longer propagation delay

So we use the product to characterize digital logic gates

$$PD = P_{\text{DISS}}(\text{avg}) \times t_p(\text{avg})$$ joules