Description: This course introduces students to hierarchical modular design of digital systems, design modeling with a hardware description language (VHDL), functional and timing simulation of digital systems, implementation in programmable logic devices and field-programmable gate arrays, formal verification, fault models and testing. Designs are developed, simulated and implemented in field programmable gate arrays (FPGAs) in laboratory sessions.

Outcomes: At the end of this course the student should be able to:

1) Understand how to describe a digital system using a Hardware Description Language (VHDL).
2) Understand and use combinational logic circuits.
3) Understand how Finite State Machines work and Design them using a Hardware Description Language.
4) Understand the HDL design flow.
5) Understand how analog effects limit the performance of digital systems.
6) Simulate digital systems and Prototype them on an FPGA (upon availability).

Instructor: Eng. Monther Y. Abusultan
Department of Computer Engineering, IUG
masltn@gmail.com

Time & Location: M Lecture (ECOM 4311-101), SuTu, 8:00am – 9:30am, K417
F Lecture (ECOM 4311-102), SuTu, 9:30am – 11:00am, N503


Website: http://site.iugaza.edu.ps/mabusultan/courses/fall-2011/ecom4311-digital-systems-design/

The website will be the main source of information for the course. All handouts, homework, and announcements will be posted. It is the student’s responsibility to download and print the necessary documents needed in the course.

Office Hours: SaMW 10:00-11:00, 13:00-14:00, 14:00-15:00
SuTu 11:00-12:00, 12:00-13:00
Also available through email appointment
Grading:

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<tr>
<th></th>
<th>Distribution</th>
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<th>(Homework &amp; Quizes)</th>
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<tbody>
<tr>
<td>Discussion</td>
<td>20%</td>
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<td>Midterm</td>
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<td>Final Project/Paper</td>
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<td>Final Exam</td>
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Notes:
- **Homework is due at the beginning of class.** Late Assignments can be turned in up to one week after the due date to receive up to 50% credit. Assignments over one week late will not receive credit.
- No make up exams will be given. Make plans to attend the exams listed above.

General Outline:
1) VHDL
2) Combinational Logic Blocks
3) Finite State Machines
4) System Design
5) System Performance
6) Design Re-Use

Academic Policies:
This course will follow the policies of the Islamic University of Gaza.
Any cheating case will be seriously dealt with by the Instructor of the course, the Department Head, and the Academic Affairs at the University. Cheating includes but is not limited to:
- **Plagiarism and copying** others’ works without proper citation (including your peers*).
- Cheating in Exams, no matter what the mean was.
- Using solution books.

* Peers are allowed to work together on solving a problem, but the final solution should be individually presented.