Introduction

This lab is a simple introduction to VHDL language and Active-HDL, the tool used for simulating the written VHDL code.

The goal of this lab is to give you, an easy start to the lab environment used in this course.

Getting Started

1) Starting Active-HDL

Note: The version that will be used in lab is Active-HDL 8.1

To start the program, go to the Start/Programs >> Aldec >> Active-HDL 8.1. The Active-HDL should start loading, which is indicated by The Active-HDL Welcome screen.
When the loading process finishes, the following dialog appears

![Getting Started Window](image)

The *Getting Started* Window.

Select the **Create new workspace** option and click the **OK** button

2) **Creating a New Workspace & Adding a new Design**

In the first wizard dialog, you should specify the name, in this case “*Lab 0*”, and location of the workspace you are creating. By default, a new design is added to this workspace.
3) Creating a New Design

After that, select the **Create an empty design** option from the *New Design Wizard*, and then click **Next**.
The next window specifies additional information about the new design, click **Next**.
The Property page

4) Entering the Design Name

The following window is the New Design Wizard, in which you should specify the name and location of this design. For example, First Design.
Finally, the last window gives a summary of this process, click **Finish**.
5) Design Browser

The Design Browser is a window showing the design contents. As a result of the previous operations it will display the following contents:
As you can see in the figure above, the design name is **First Design**. In order to add a VHDL source file right click on the Add New File item, select New and then VHDL Source. The New Source File wizard starts, click Next.

![New Source File Wizard](image)

**The New Source File wizard**

Type the name of the source file, as an example: **NandGate**, press **Next**, then **Finish**.

![New Source File Wizard - Name](image)
Compile the source file by choosing the **Compile** option from the shortcut menu. To invoke the menu, click with the right mouse button over the file name or press **F11**.

After successful compilation, the “✓” icon will appear close to the file name along with the “!” sign allowing the expansion of the design structure.

If the source file contains an error, the “!” sign appears at the file name. Erroneous line is underlined and the VHDL console window displays the error description.

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The window shows an entity-architecture pair.

6) **Code Editing: HDL Editor**

The **HDL Editor** is a text editor with HDL keywords coloring and standard editing features. Active-HDL offers another useful feature that allows grouping, collapsing and expanding particular VHDL constructs to improve readability of the code.
7) Simulation, getting start

To begin a simulation, you have to generate a test file that is called a “TestBench”. This could be done by right click to the entity-architecture pair, in this case the `nandgate(behavior)`, select from the menu Generate TestBench.

```vhdl
library IEEE;
use IEEE.STD_LOGIC_1164.all;

entity NandGate is
  PORT
  (    A: IN BIT;
    B: IN BIT;
    Q: OUT BIT -- Note! No ';' ' here!
  );
end NandGate;

--)) End of automatically maintained section
architecture behaviour of NandGate is
SIGNAL temp: BIT;
begin
  temp <= A AND B; -- The AND-operation.
  Q <= NOT temp;  -- The inverter.

  -- enter your statements here --
end behaviour;
```
Follow the wizard by pressing **Next**.
Select the design unit for which you want to generate a testbench. The wizard will generate appropriate source files and a macro file for the testbench.

Entity:

random

Architecture:

behaviour

Testbench Type:
- [ ] Single Process
- [ ] WAVES Based
- [ ] Alesc TestBench
Click Next, then specify the testbench specifications as shown below and click Next then Finish.
This wizard offers you a template for the desired testbench all you have to do is to write a simulation process that tests the behavior of the design. This testbench appears under the Structure tab of the Design Browser window as follows. Compile the testbench file.

Add this lines to simulate input values

\[
\begin{align*}
a & \leftarrow '0', \\
'b' & \text{ AFTER 10 ns,} \\
'0' & \text{ AFTER 30 ns,} \\
'b' & \text{ AFTER 40 ns;} \\
b & \leftarrow '0', \\
'0' & \text{ AFTER 10 ns,} \\
'b' & \text{ AFTER 30 ns,} \\
'b' & \text{ AFTER 40 ns;}
\end{align*}
\]
After successful compilation you have to initialize the simulator first, using the **Initialize Simulation** option from the **Simulation** menu.

After the simulator has been initialized, you have to open a new **Waveform** window. Click the **New Waveform** toolbar button. The new **Waveform** window appears.

*After compiling testbench file*
To add signals to the simulator, use the drag-and-drop method. Open the Structure tab of the Design Browser window, select the testbench file just created and while holding down the left button, drag it to the right-section of the waveform window and then release the mouse button. This is a standard drag-and-drop operation.
Adding Signals From Design Browser Window

If you want to delete a signal, select it and press the Del button.

Active-HDL allows inspection of simulation results in the tabled format with delta time precision. The List Viewer window enables signal values monitoring without the ability to force signals with the desired values. To open the Viewer window click the New List toolbar button. The window below will appear as a result.
The List Viewer window is an interactive display which mirrors all simulation actions and results.

8) Let's simulate

Perform several simulation steps by clicking the Run button. You will receive the following results on the Waveform tab.

The Simulation Results
Choose **End Simulation** from the **Simulation** menu. Save the waveform under the file name: *Waveform Editor 1.awf*.

To display the results in the tabled format and monitor delta time changes switch to the opened List Viewer window. The results should be displayed in the similar manner.

<table>
<thead>
<tr>
<th>Time</th>
<th>Delta</th>
<th>UUT/amp</th>
<th>UUT/A</th>
<th>UUT/B</th>
<th>UUT/Q</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 ps</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0 ps</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>20000 ps</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>40000 ps</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>60000 ps</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>60000 ps</td>
<td>2</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

*Simulation results in the List Viewer*