Introduction

This lab’s objective is to demonstrate how to use FSM.

Question 1

Let’s design a 2-bit Up/Down Gray Code Counter using User-Enumerated State Encoding

- In=0, Count Up
- In=1, Count Down
- this will be a Moore or Mealy? which is easier?
- no Reset

Question 2

Implement a sequence detector for “10110” and test your work
Question 3

Write VHDL code that Describe this FSM design…

Question 4

Generate the following signal

```
clk

outp
```
Homework

1- Generate the following two signals

2- You are to design a “Serial Sequence Detector”. Your design will take in a clock, reset, and a one-bit data signal. Your design will check the input data signal on the rising edge of the input clock. When it finds the sequence “01100110”, it will assert an output signal “Found” for one clock cycle (important).